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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,305	02/28/2002	Stephen M. Trimberger	X-874 US	7532

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,305	TRIMBERGER, STEPHEN M.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a Non-Final Office Action in response to Amendment filed 11/29/2004. Claims 1-39 are pending and are hereby presented for examination.

The objection to the drawings is hereby withdrawn in view of the amendment to the drawings as shown in the replacement sheets.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Charlton et al. (US Patent NO: 6,289,292, issued: September 11, 2001, filed: October 28, 1997).

Regarding independent Claims 1, 25, Charlton discloses a system and a method for identification of electronic components based on their physical characteristics, including a characterization value test station for determining the characterization values of the components pursuant to the characterization function, and a data base

which stores information that pertains to each component with the component's characterization value linked as an identifier to the information, wherein information pertaining to a component may be retrieved from the database based on the component's characterization value, see Abstract and Summary of the Invention, comprising:

Testing a plurality of memory devices (16a-d) of memory 15 in a memory module, Figures 2 and 5, and for each memory device 16 from a set of memory devices (16a-d), using the memory tester to determine a device's characterization value and tests the device for bit defects.

Recording defect data for each defective memory device (16a-d), wherein as disclosed, "the bit defect information and characterization value are stored together in a database record to link the characterization value as an identifier to the bit defect information. After all of the devices have been tested and linked to their characterization value, they can then be combined and distributed for manufacturing or other processes without requiring any added marks or identification materials".

Receiving and providing from and to a user, respectively, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

With respect to programmable logic devices (PLD) being under test, according to Charlton Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Regarding independent Claims 9, 33, Charlton discloses the common limitations as described in the independent claim 1, above, comprising:

Receiving and providing from and to a user, respectively, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

With respect to programmable logic devices (PLD) being under test, according to Charlton Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

In addition, Charlton discloses implementing the user design, in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding independent Claim 20, Charlton discloses the common limitations as described in the independent claim 1, above, comprising:

Testing a plurality of memory devices (16a-d) of memory 15 in a memory module, Figures 2 and 5, and for each memory device 16 from a set of memory devices (16a-d), using the memory tester to determine a device's characterization value and tests the device for bit defects.

Recording defect data for each defective memory device (16a-d), wherein as disclosed, "the bit defect information and characterization value are stored together in a database record to link the characterization value as an identifier to the bit defect information. After all of the devices have been tested and linked to their characterization value, they can then be combined and distributed for manufacturing or other processes without requiring any added marks or identification materials".

Receiving and providing from and to a user, respectively, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

With respect to programmable logic devices (PLD) being under test, according to Charlton Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

In addition, Charlton discloses implementing the user design, in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claims 2, 10, 21, 26, 34, Charlton discloses receiving an identifier (component's characterization value) from a user (manufacturer), and providing to the manufacturer the component's bit defect information from the database via the data communications link, which is the link between the characterization value test station 50 and a personal computer 35 for monitoring and controlling test station 50.

Regarding Claims 3, 4, 11, 12, Charlton discloses wherein the location information, such as the bit error information (i.e., defect locations) of memory 15 is available to memory recovery interface 12, which provides to host processor 14 access to memory 15 without alteration of the processor's addressing scheme, while preventing any defective memory cells/bytes of memory 15 from being used. The bit error information is provided to memory recovery interface 12 through EPROM 13 (e.g., the information could be downloaded into internal memory of memory recovery interface 12 during start-up).

Regarding Claims 5, 13, 27, Charlton discloses implementing a user design in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored,

then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claims 6, 28, 35, Charlton discloses receiving and providing from and to a user, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

Regarding Claims 7, 16, 23, 29, 36, Charlton discloses with respect to a PLD being field programmable gate array (FPGA), according to Charlton Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Regarding Claims 8, 17, 24, Charlton discloses maintaining the database for storing the bit defect information and the characterization value which links the characterization value as an identifier to the bit defect information, including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Regarding Claims 14, 15, Charlton discloses receiving and providing from and to a user, such as a manufacturer, an identifier corresponding to the component's

characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

Implementing a user design in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claim 18, Charlton discloses with respect to a PLD being field programmable gate array (FPGA), according to Charlton Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Implementing a user design in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claim 19, Charlton discloses implementing the user design in a defective memory device (16a-d), including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Regarding Claim 22, Charlton discloses receiving and providing from and to a user, respectively, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

Implementing the user design, in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claims 30-32, 37-39, Charlton discloses device specific information comprising a database for storing the bit defect information and the characterization value which links the characterization value as an identifier to the bit defect information, including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Response to Arguments

3. Applicant's arguments, see AMENDMENT, filed 11/29/2004, with respect to the rejections of claims 1, 3-9, 11, 12, 14, 16-19, 25, 27- 29, 31-33, 35, 36, 38 and 39 rejected under 35 U.S.C. 102(b) as being anticipated by McClintock et al. (US Patent No: 6,166,559), and claims 2, 10, 13, 15, 20-24, 26, 30, 34 and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over McClintock et al. (US Patent No: 6,166,559) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of claims 1-39 rejected under 35 U.S.C. 102(e) as being anticipated by Charlton et al. (US Patent NO: 6,289,292), as set forth in the present Office Action.

4. In reference to claims rejected under 35 U.S.C. 102(b) as being anticipated by McClintock et al. (US Patent No: 6,166,559), the Examiner agrees with the Applicant that McClintock fails to disclose the limitations, as to independent claims 1, 9, 20, 25 and 33, related to recording data for each PLD (either defect data or device specific data), the data including a unique identifier for each PLD; maintaining a database of the device data; receiving a first identifier from a user; providing to the user device data from the database corresponding to the first identifier and obtaining device-specific data used in implementing the design. However, under new grounds of rejection, Charlton et al. (US Patent NO: 6,289,292) anticipates the above limitations recited in the independent claims 1, 9, 20, 25 and 33.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Date: 15 March 2005
Office Action: Non-Final Rejection

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